

## United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

DATE MAILED: 10/29/2002

<u> </u>				
APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/490,132	01/24/2000	William C. Moyer	SC10927TS	6776
759	00 10/29/2002			
Harry A Wolin			EXAMINER	
Motorola INc Austin Intellectual Property 7700 West Parmer lane			HUYNH, KIM T	
MD TX32/PL02 Austin, TX 78729			ART UNIT	PAPER NUMBER
			2189	

Please find below and/or attached an Office communication concerning this application or proceeding.

1

,		Application No.	Applicant(s)
Office Action Summary		09/490,132	MOYER, WILLIAM C.
		Examiner	Art Unit
		Kim T. Huynh	2189
Period fo	The MAILING DATE of this communication apport	pears on the cover sheet with the	correspondence address
- Exte after - If the - If NC -, Failu - Any I	IORTENED STATUTORY PERIOD FOR REPL MAILING DATE OF THIS COMMUNICATION. ensions of time may be available under the provisions of 37 CFR 1.1 SIX (6) MONTHS from the mailing date of this communication. e period for reply specified above is less than thirty (30) days, a reply operiod for reply is specified above, the maximum statutory period for reply within the set or extended period for reply will, by statute reply received by the Office later than three months after the mailing ed patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply be ti y within the statutory minimum of thirty (30) da will apply and will expire SIX (6) MONTHS from	mely filed ys will be considered timely. In the mailing date of this communication.
1)[7]	Responsive to communication(s) filed on Sep	tember 3, 2002 .	
2a)□		is action is non-final.	
3)☐ Dispositi	Since this application is in condition for allowa closed in accordance with the practice under on of Claims	ance except for formal matters in	rosecution as to the merits is 453 O.G. 213.
4)🖂	Claim(s) $\underline{1-16}$ is/are pending in the application		
-	4a) Of the above claim(s) is/are withdrav	vn from consideration.	
5)	Claim(s) is/are allowed.		
6)🖂	Claim(s) <u>1-16</u> is/are rejected.		
7)	Claim(s) is/are objected to.		
8)	Claim(s) are subject to restriction and/or	election requirement.	
l _	on Papers		
∫ 9)□ T	The specification is objected to by the Examiner		
10)□ T	he drawing(s) filed on is/are: a)□ accept	ted or b)⊡ objected to by the Exar	miner.
	Applicant may not request that any objection to the	drawing(s) be held in abeyance. Se	ee 37 CFR 1.85(a).
11)∐ T 	he proposed drawing correction filed on		ved by the Examiner.
40) 🗆 –	If approved, corrected drawings are required in repl		
	he oath or declaration is objected to by the Exa	miner.	
	nder 35 U.S.C. §§ 119 and 120		
13) 🗌 🛭	Acknowledgment is made of a claim for foreign	priority under 35 U.S.C. § 119(a)	-(d) or (f) March De
a) <u></u>	] All b) ☐ Some * c) ☐ None of:		DI IPAI DHARIA
1	1. ☐ Certified copies of the priority documents	have been received.	PRIMARY EXAMINER
2	2. Certified copies of the priority documents	have been received in Application	on No
	B. Copies of the certified copies of the priorit application from the International Bure the attached detailed Office action for a list of	y documents have been received	d in this National Stage
	knowledgment is made of a claim for domestic		
a) [	☐ The translation of the foreign language provi knowledgment is made of a claim for domestic	sional application has been rece	ived.
1) Notice of 2) Notice of 3) Informa	of References Cited (PTO-892) of Draftsperson's Patent Drawing Review (PTO-948) tion Disclosure Statement(s) (PTO-1449) Paper No(s)	4) Interview Summary ( 5) Notice of Informal Pa 6) Other:	PTO-413) Paper No(s) atent Application (PTO-152)
S. Patent and Trade PTO-326 (Rev.		on Summary	Part of Paper No. 2

Art Unit: 2189

#### **DETAILED ACTION**

# Notice to Applicant(s)

1. This application has been examined. Claims 1-16 are pending.

#### Response to Arguments

2. Applicant's arguments with respect to claims 1-16 have been considered but are deemed to be moot in view of the new grounds of rejection.

## Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 4. Claims 1-4, 6 and 9-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Arndt et al. (U. S Patent 5,701,495)

### Arndt discloses:

- a. As per claims 1,9 and 14,
  - providing a first storage device having a plurality of inputs, each of
    the plurality of inputs being coupled by a respective physical
    conductor to one of a plurality of hardware-generated interrupt
    sources which selectively generate hardware interrupts and
    selectively storing the hardware interrupts, the first storage device

Art Unit: 2189

Page 3

providing one or more hardware-generated interrupt signals. (col.18, lines 28-32)

- providing a second storage device having one or more inputs, each of the one or more inputs receiving and storing a predetermined one of a plurality of software-generated interrupt signals, at least some of the predetermined plurality of software-generated interrupt signals indicating an interrupt from a different source or of a different type than the hardware interrupts, the second storage device providing one or more software-generated interrupt signals (col.8, lines 56-67), (col.9, lines 1-13), (col.18, lines 20-27), (col.2, lines 26-43), (col.4, lines 27-32), (see abstract, lines 3-13)
- coupling logic circuitry to the first storage device and the second storage device for receiving the one or more hardware-generated interrupt signals and the one or more software-generated signals, the logic circuitry providing an interrupt request signal which will cause an interrupt to occur in the data processing system (col.4, lines 25-35), (col.9, lines 14-17)
- a plurality of hardware interrupt sources; (col.18, lines 28-32)
- executing software with the data processing system to generate a
  predetermined software-generated interrupt signal which emulates
  a predetermined one of the hardware-generated interrupt sources
  but with a priority which differs from the predetermined one of the

Art Unit: 2189

hardware-generated interrupt sources, thereby dynamically changing prioritization of servicing of interrupts in the data processing system; (col.9, lines 15-67), (col.10, lines 1-67), (col.11, lines 1-14)

- b. As per claims 2 and 10, assigning an interrupt prioritization level to specific storage locations of the first storage device and the second storage device, the interrupt prioritization level of the plurality of hardware-generated interrupt source coupled to the first storage device being permanently assigned, but assignment of the interrupt prioritization level of interrupt sources associated with the second storage device being variable by software control. (col.4, lines 27-32), (col.4, lines 53-61), (col.2, lines 26-43).
- c. As per claim 3, assigning a portion of the plurality of software-generated interrupt signals stored in the second storage device to represent interrupts from some interrupt sources generating hardware interrupt and having a corresponding interrupt prioritization level (col.3, lines 36-68), (col.4, lines 1-67).

  d. As per claim 4, assigning a portion of the plurality of software-generated interrupt signals stored in the second storage device to represent interrupts from same interrupt sources generating hardware interrupts and having an interrupt prioritization level which differs from the interrupt prioritization level of the plurality of hardware-generated interrupt sources coupled to the first storage device (col.4, lines 17-32)

Art Unit: 2189

e. As per claim 6, changing prioritization level of a predetermined hardware-generated interrupt by providing a software-generated interrupt which represents a corresponding hardware-generated interrupt source for the predetermined hardware-generated interrupt but with a different prioritization level than the predetermined hardware-generated interrupt. (col.12, lines 56-65), (col.9, lines 52-67), (col.10, lines 1-9)

- f. As per claim 11, a software-generated interrupt signal of higher priority than a currently executing hardware-generated interrupt signal is provided to the logic circuitry prior to completion of an associated hardware interrupt servicing, and the data processing system suspends processing of the hardware interrupt servicing to process an associated software interrupt servicing. (col.9, lines 15-67), (col.10, lines 1-53), (col.12, lines 10-31)
- g. As per claims 12 and 16, a mask register coupled to the hardware interrupt storage device and the software interrupt storage device for selectively preventing hardware-generated interrupt signals and software-generated interrupt signals from propagating to the logic circuitry. (col.12, lines 10-31) h. As per claim 13, the hardware interrupt storage device and the software interrupt storage device are each implemented as latch circuits. (col.4, lines 53-61)
- i. As per claim 15, generating the predetermined software-generated interrupt signal which emulates the predetermined one of the hardware-generated interrupt sources while another hardware-generated interrupt is being serviced,

Art Unit: 2189

the predetermined software-generated interrupt signal having a priority which is higher than the other hardware-generated interrupt being serviced; (col.9, lines 15-67), (col.10, lines 1-67), (col.11, lines 1-13)

# Claim Rejections - 35 USC § 103

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. Claims 5,7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arndt et al. (U.S Patent 5,701,495) in view of Koscal et al. (U.S Patent 6,412,081)

Arnedt discloses all the limitations as above except the limitation that the changing interrupt servicing from hardware-generated to software-generated interrupt, combination circuitry to determining whether to pass the hardware-generated and software-generated interrupts and determining priority between two interrupts as claimed as claims 5,7 and 8.

However, Koscal discloses a predetermined bit of the PSR is placed in a defined state responsive to the occurrence of a condition. (see abstract, lines 8-25), Furthermore, the output of the compare circuit changes state whenever the data matches value, depending on the specific implementation. (col.7, lines 49-63). The particular state of the bit is determined the responsive to whether an interrupt is a hardware or software interrupt. (col.9, lines 52-67), (col.10, lines 1-13)

It would have been obvious one having ordinary skills in the art at the time the invention was made to incorporate Koscal's teaching into Arndt's method to include the changing interrupt servicing from hardware-generated to software-generated interrupt, combination circuitry to determining whether to pass the hardware-generated and software-generated interrupts and determining priority between two interrupts as to be a greater flexibility and compatible with the latest advancements in the computer system technology.

#### Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sleeman et al. [USPN 6,397,284] discloses apparatus and method for handling peripheral device interrupts.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM-6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor,

Peter Wong can be reached on (703)305-3477 or via e-mail addressed to [Peter.Wong@uspto.gov]. The
fax phone numbers for the organization where this application or proceeding is assigned are (703)7467249 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

Oct. 25, 2002

RUPAL DHARIA PRIMARY EXAMINER